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EXAMINER	
GOGIA, ANKUR	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,984	JEDDELOH, JOSEPH M.	
	Examiner	Art Unit	
	Ankur Gogia	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/29/03, 5/14/04*. & 7/14 104
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application, having Application No. 10/747,984, has a total of 34 claims pending in the application; there are 4 independent claims and 30 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

3. As required by M.P.E.P. 609(c), the applicant's submission of the Information Disclosure Statements dated 29 December 2003, 14 May 2004 and 14 July 2004 is acknowledged by the examiner and the cited references, with the exception of citation AS on the IDS dated 14 May 2004, have been considered in the examination of the claims now pending. As required by M.P.E.P. 609(c)(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

4. With regards to citation AS on the IDS dated 14 May 2005, the applicant cites pgs. 1-178, the entire document, as being pertinent. Examiner respectfully requests if the applicant may provide a narrower citation of the relevant pages of the document.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claims 1, 10, 11, 19, 21, 30, 31 and 33 disclose "to couple memory requests" or "coupling of memory requests". Generally the term "couple" is used to designate that one device or system is connected to another device or system. The examiner is unsure how a request would be "coupled to" a device or system. More appropriate terminology may be "transmit(ting)" rather than "couple(ing)". For the purposes of this office action, the examiner will interpret "couple(ing)" as used in claims 1, 10, 11, 19, 21, 30, 31 and 33 as meaning "transmit(ting)". All other claims not specifically discussed are rejected for inheriting the deficiencies of the claims from which they depend.

Claim Rejections - 35 USC § 103

7. Claims 1, 3, 7-10, 11, 13, 17-20 and 31-34 are rejected under 35 U.S.C. 103(a) as being obvious over Holman (6,970,968) in view of Soejima et al. (2004/0123180).

Independent Claim 1

Holman discloses a memory module **(Fig. 3, Item 306; Col. 4, Line 33)**, comprising:

a plurality of memory devices **(Fig. 3, Items 312-315; Col. 4, Lines 47-51)**; and

a memory hub **(Fig. 3, Item 310; Col. 4, Lines 47-48)**, comprising

a link interface receiving memory requests for access to memory cells in at least one of the memory devices **(Fig. 8, Item 804; Col. 9, Lines 6-7)**

a memory device interface coupled to the memory devices **(Fig. 8, Items 802, 830, 832, 834, 836 make up the interface to the memory devices as these are the elements that generate and output the appropriate signals for the memory devices; Col. 9, Lines 1-7 and 17-33)**, the memory device interface being "operable to" couple **(interpreted as "transmit"; see ¶6 above)** memory requests to the memory devices for access to the memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests **(Col. 9, Lines 1-7 and 17-33; requests may be reads or writes)**.

Holman does not disclose expressly wherein the memory hub comprises

a performance counter coupled to the memory device interface, the performance counter operable to track at least one performance metric.

Soejima et al. disclose performance information management units that manage the performance of storage devices through the collection of various performance metrics including total number of requests, average request processing interval, total transfer amount and average transfer rate **(Figs. 4, 5, 9; ¶s 72, 74, 97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to

incorporate a performance measurement unit in a memory device to measure various performance metrics of the memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 1.

Independent Claim 11

Holman discloses a memory hub **(Fig. 3, Item 310; Col. 4, Lines 47-48)**, comprising:

a link interface receiving memory requests for access to memory cells in at least one of the memory devices **(Fig. 8, Item 804; Col. 9, Lines 6-7)**

a memory device interface coupled to the memory devices **(Fig. 8, Items 802, 830, 832, 834, 836 make up the interface to the memory devices as these are the elements that generate and output the appropriate signals for the memory devices; Col. 9, Lines 1-7 and 17-33)**, the memory device interface being operable to couple **(interpreted as "transmit"; see ¶6 above)** memory requests to the memory devices for access to the memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests **(Col. 9, Lines 1-7 and 17-33; requests may be reads or writes)**.

Holman does not disclose expressly wherein the memory hub comprises

a performance counter coupled to the memory device interface, the performance counter operable to track at least one performance metric.

Soejima et al. disclose performance information management units that manage the performance of storage devices through the collection of various performance metrics including total number of requests, average request processing interval, total transfer amount and average transfer rate **(Figs. 4, 5, 9; ¶s 72, 74, 97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit in a memory device to measure various performance metrics of the memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 11.

Claims 3 and 13

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claims depend, as discussed above.

Holman further discloses wherein the memory device interface comprises a memory controller **(Fig. 8, Item 802; Col. 9, Lines 17-33)**.

Holman does not disclose expressly wherein the performance counter is coupled to the memory controller.

Soejima et al. disclose a performance information management unit coupled to a CPU **(Fig. 4)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit coupled to a memory controller in a memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claims 3 and 13.

Claims 7 and 17

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claims depend, as discussed above.

Holman does not disclose expressly wherein the performance counter is further coupled to the link interface.

Soejima et al. disclose in Figs. 2 and 3 systems in which a computer transmits requests and data to a storage device. The storage devices contain a performance

information management unit as shown in Fig. 4 that is connected to a CPU and a communication device that process requests and as shown in Fig. 4 the performance information management unit is coupled to the CPU and communication device.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit coupled to a memory controller in a memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claims 7 and 17.

Claims 8 and 18

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claims depend, as discussed above.

Holman does not disclose expressly wherein the performance metric tracked by the performance counter comprises at least one performance metric selected from the group consisting of page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests,

rate or percentage or memory bus utilization, local hub request rate or number and remote hub request rate or number.

Soejima et al. disclose a system for performance monitoring of a storage device wherein the performance information management unit tracks the total number of requests **(number of read/write requests)**, average request processing interval **(read/write rate)** and average transfer rate **(local hub request rate)** associated with the local storage devices **(Figs. 9 and 10; ¶97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit coupled to a memory controller in a memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claims 8 and 18.

Claims 9 and 20

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claims depend, as discussed above.

Holman further discloses wherein the memory devices comprise dynamic random access memory devices **(Fig. 5; Col. 7, Lines 24-38)**.

Claims 10 and 19

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claims depend, as discussed above.

Holman does not disclose expressly wherein the performance metric tracked by the performance counter comprises a performance metric related to the coupling of memory requests and data through the memory hub.

Soejima et al. disclose a system for measuring performance of storage devices wherein the performance metrics measured are metrics relating to the transmission of requests and data **(Figs. 9 and 10; ¶s 72, 74 and 97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit in a memory device to measure various performance metrics of the memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claims 10 and 19.

Independent Claim 31

Holman discloses a method of reading data from a memory module **(Fig. 3, Item 306; Col. 4, Line 33)**, comprising:

receiving memory requests for access to a memory device mounted on the memory module **(Fig. 8, Item 804; Col. 9, Lines 6-7)**;

coupling the memory requests to the memory device responsive to the received memory request, at least some of the memory requests being memory requests to read data; **(Col. 9, Lines 1-4, 60-63)**

receiving read data responsive to the read memory requests **(Col. 9, Lines 60-63)**.

Holman does not disclose expressly wherein the method comprises

tracking at least one performance metric within the memory module.

Soejima et al. disclose performance information management units that manage the performance of storage devices through the collection of various performance metrics including total number of requests, average request processing interval, total transfer amount and average transfer rate **(Figs. 4, 5, 9; ¶s 72, 74, 97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit in a memory device to measure various performance metrics of the memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 31.

Claim 32

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claim depends, as discussed above.

Holman does not disclose expressly wherein the act of tracking at least one performance metric comprises tracking at least one performance metric selected from the group consisting of page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests, rate or percentage of memory bus utilization, local hub request rate or number and remote hub request rate or number.

Soejima et al. disclose a system for performance monitoring of a storage device wherein the performance information management unit tracks the total number of requests **(number of read/write requests)**, average request processing interval **(read/write rate)** and average transfer rate **(local hub request rate)** associated with the local storage devices **(Figs. 9 and 10; ¶97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit coupled to a memory controller in a memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 32.

Claim 33

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claim depends, as discussed above.

Holman does not disclose expressly wherein the act of tracking at least on performance metric comprises tracking a performance metric related to the coupling of memory requests and data through the memory hub.

Soejima et al. disclose a system for measuring performance of storage devices wherein the performance metrics measured are metrics relating to the transmission of requests and data **(Figs. 9 and 10; ¶s 72, 74 and 97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to

incorporate a performance measurement unit in a memory device to measure various performance metrics of the memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 33.

8. Claims 2, 12 and 34 are rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. as applied to claims 1, 11 and 31 above, and further in view of Henderson et al. (5,274,584).

Claims 2 and 12

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claims depend, as discussed above.

They do not disclose expressly wherein the link interface comprises an optical input/output port.

Henderson et al. disclose a solid state memory device having an optical data connection between the memory device and read/write devices **(Col. 1, Lines 9-13)**.

The combination of Holman and Soejima et al. and Henderson et al. are analogous art because they are from the similar problem solving area of a memory device with improved data transfer rate.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman and Soejima et al. and Henderson et al. before them, to include an optical link to a memory device.

The motivation for doing so would have been to avoid the mechanical degradation associated with electrical connectors **(Henderson et al. Col. 2, Lines 34-37)**.

Therefore, it would have been obvious to combine Henderson et al. with the combination of Holman and Soejima et al. for the benefit of avoiding mechanical degradation to obtain the invention as specified in claims 2 and 12.

Claim 34

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claim depends, as discussed above.

They do not disclose expressly wherein the act of receiving memory requests for access to a memory device mounted on the memory module comprises receiving optical signals corresponding to the memory requests.

Henderson et al. disclose a solid state memory device having an optical data connection between the memory device and read/write devices **(Col. 1, Lines 9-13)**.

The combination of Holman and Soejima et al. and Henderson et al. are analogous art because they are from the similar problem solving area of a memory device with improved data transfer rate.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman and Soejima et al. and Henderson et al. before them, to include an optical link to a memory device.

The motivation for doing so would have been to avoid the mechanical degradation associated with electrical connectors **(Henderson et al. Col. 2, Lines 34-37)**.

Therefore, it would have been obvious to combine Henderson et al. with the combination of Holman and Soejima et al. for the benefit of avoiding mechanical degradation to obtain the invention as specified in claim 34.

9. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. as applied to claims1 and 11 above, and further in view of Fukuda et al. (5,619,676).

Claims 4 and 14

The combination of Holman and Soejima et al. discloses claims 1 and 11 as above and further discloses wherein the memory device interface comprises a cache **(Holman Fig. 10, Items 1012 and 1038; Col. 11, Lines 36-40, 44-46 and 49-51)**.

The combination of Holman and Soejima et al. does not disclose expressly wherein the performance counter is further coupled to the cache.

Fukuda et al. disclose a memory module including a cache and a counter to track the hit ratio of the cache **(Fig. 1; Abstract, Col. 7, Lines 3-9)**.

The combination of Holman and Soejima et al. and Fukuda et al. are analogous art because they are from the similar problem solving area of improving performance of a memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman and Soejima et al. and Fukuda et al. before them, to attach a performance counter to a cache.

The motivation for doing so would have been to improve the performance of the cache and memory **(Fukuda et al. Col. 3, Line 65 – Col. 4, Line 2)**.

Therefore, it would have been obvious to combine Fukuda et al. with the combination of Holman and Soejima et al. for the benefit of improved cache and memory performance to obtain the invention as specified in claims 4 and 14.

10. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. as applied to claims 1 and 11 above, and further in view of Rotithor et al. (2004/0123043).

Claims 5 and 15

The combination of Holman and Soejima et al. discloses claims 1 and 11 as above and further discloses wherein the memory hub further comprises a prefetch buffer **(Holman Fig. 8, Item 812; Col. 9, Lines 59-63)**.

The combination of Holman and Soejima et al. does not disclose expressly wherein the performance counter is further coupled to the prefetch buffer.

Rotithor et al. disclose wherein a performance counter is coupled to a prefetch buffer **(Fig. 2)**.

The combination of Holman and Soejima et al. and Rotithor et al. are analogous art because they are from the similar problem solving area of improving performance on a memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman and Soejima et al. and Rotithor et al. before them, to attach a performance counter to a prefetch buffer.

The motivation for doing so would have been maximizing the performance of applications **(Rotither et al. ¶8)**.

Therefore, it would have been obvious to combine Rotithor et al. with the combination of Holman and Soejima et al. for the benefit of improved performance of applications to obtain the invention as specified in claims 5 and 15.

11. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. as applied to claims 1 and 11 above, and further in view of Battaline et al. (5,768,152).

Claims 6 and 16

The combination of Holman and Soejima et al. discloses the limitation of the claims(s) upon which the instant claims depend, as discussed above.

The combination of Holman and Soejima et al. does not disclose expressly wherein the memory hub further comprises a maintenance bus, and the performance counter is further coupled to the maintenance bus.

Battaline et al. disclose a system for providing performance analysis on integrated circuit devices using an IEEE JTAG 1149.1 interface.

The combination of Holman and Soejima et al. and Battaline et al. are analogous art because they are from the similar problem solving area of improving performance of an integrated circuit device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of he combination of Holman and Soejima et al. and Battaline et al. before them, to incorporate a maintenance bus such as the JTAG interface into a system for performance monitoring in a memory device.

The motivation for doing so would have been to monitor the performance of the integrated circuit device without compromising the system performance **(Battaline et al. Col. 1, Lines 43-46)**.

Therefore, it would have been obvious to combine Battaline et al. with the combination of Holman and Soejima et al. for the benefit of system monitoring without performance degradation to obtain the invention as specified in claims 6 and 16.

12. Claims 21, 23 and 27-30 are rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. and applicant's admitted prior art (hereinafter referred to as AAPA).

Independent Claim 21

Holman discloses a memory module **(Fig. 3, Item 306; Col. 4, Line 33)**, comprising:

a plurality of memory devices **(Fig. 3, Items 312-315; Col. 4, Lines 47-51)**; and

a memory hub **(Fig. 3, Item 310; Col. 4, Lines 47-48)**, comprising

a link interface receiving memory requests for access to memory cells in at least one of the memory devices **(Fig. 8, Item 804; Col. 9, Lines 6-7)**

a memory device interface coupled to the memory devices **(Fig. 8, Items 802, 830, 832, 834, 836 make up the interface to the memory devices as these are the elements that generate and output the appropriate signals for the memory devices; Col. 9, Lines 1-7 and 17-33)**, the memory device interface being operable to couple **(interpreted as "transmit"; see ¶6 above)** memory requests to the memory devices for access to the memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests **(Col. 9, Lines 1-7 and 17-33; requests may be reads or writes)**.

Holman does not disclose expressly wherein the memory hub comprises

a performance counter coupled to the memory device interface, the performance counter operable to track at least one performance metric.

Furthermore, Holman does not disclose expressly wherein the memory hub is implemented in a computer system comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices; and

the memory hub.

Soejima et al. disclose performance information management units that manage the performance of storage devices through the collection of various performance metrics including total number of requests, average request processing interval, total transfer amount and average transfer rate **(Figs. 4, 5, 9; ¶s 72, 74, 97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit in a memory device to measure various performance metrics of the memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 21.

The combination of Holman and Soejima et al. does not disclose expressly a computer system comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices.

AAPA discloses on page 1, lines 8-12, a conventional computer system that comprises memory devices **(memory modules having a plurality of memory devices)**, accessed by a processor **(CPU)** which communicates with the memory devices through a processor bus and a memory controller **(System Controller)**. AAPA does not state explicitly that the computer system has input or output devices coupled to the system controller or a storage device coupled to the system controller, these are all inherent elements in a conventional computer system such as that disclosed by AAPA.

The combination of Holman and Soejima et al. and AAPA are analogous art because they are from the same field of endeavor of improving the performance of a memory module used in a typical computer system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman and Soejima et al. and AAPA before them, to incorporate the memory hub disclosed into the conventional computer system of AAPA.

The motivation for doing so would have been to optimize the configuration of the memory module **(AAPA Pg. 3, Lines 25-29)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 21.

Claim 23

Holman discloses claim 21 as above and further discloses wherein the memory device interface comprises a memory controller **(Fig. 8, Item 802; Col. 9, Lines 17-33)**.

Holman does not disclose expressly wherein the performance counter is coupled to the memory controller.

Soejima et al. disclose a performance information management unit coupled to a CPU **(Fig. 4)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit coupled to a memory controller in a memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 23.

Claim 27

Holman discloses claim 21 as above.

Holman does not disclose expressly wherein the performance counter is further coupled to the link interface.

Soejima et al. disclose a in Figs. 2 and 3 systems in which a computer transmits requests and data to a storage device. The storage devices contain a performance information management unit as shown in Fig. 4 that is connected to a CPU and a communication device that process requests and as shown in Fig. 4 the performance information management unit is coupled to the CPU and communication device.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit coupled to a memory controller in a memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 27.

Claim 28

Holman discloses claim 21 as above.

Holman does not disclose expressly wherein the performance metric tracked by the performance counter comprises at least one performance metric selected from the group consisting of page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests, rate or percentage or memory bus utilization, local hub request rate or number and remote hub request rate or number.

Soejima et al. disclose a system for performance monitoring of a storage device wherein the performance information management unit tracks the total number of requests **(number of read/write requests)**, average request processing interval **(read/write rate)** and average transfer rate **(local hub request rate)** associated with the local storage devices **(Figs. 9 and 10; ¶97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit coupled to a memory controller in a memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 28.

Claim 29

Holman further discloses wherein the memory devices comprise dynamic random access memory devices **(Fig. 5; Col. 7, Lines 24-38)**.

Claim 30

Holman discloses claim 21 as above.

Holman does not disclose expressly wherein the performance metric tracked by the performance counter comprises a performance metric related to the coupling of memory requests and data through the memory hub.

Soejima et al. disclose a system for measuring performance of storage devices wherein the performance metrics measured are metrics relating to the transmission of requests and data **(Figs. 9 and 10; ¶s 72, 74 and 97)**.

Holman and Soejima et al. are analogous art because they are from the same field of endeavor of improving the performance of a memory device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Holman and Soejima et al. before them, to incorporate a performance measurement unit in a memory device to measure various performance metrics of the memory device.

The motivation for doing so would have been to prevent the memory device from degrading **(Soejima et al. ¶260)**.

Therefore, it would have been obvious to combine Soejima et al. with Holman for the benefit of less degradation of the memory device to obtain the invention as specified in claim 30.

13. Claim 22 is rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. and AAPA as applied to claim 21 above, and further in view of Henderson et al. (5,274,584).

Claim 22

The combination of Holman, Soejima et al. and AAPA discloses claim 21 as above.

They do not disclose expressly wherein the link interface comprises an optical input/output port.

Henderson et al. disclose a solid state memory device having an optical data connection between the memory device and read/write devices **(Col. 1, Lines 9-13)**.

The combination of Holman, Soejima et al. and AAPA and Henderson et al. are analogous art because they are from the similar problem solving area of a memory device with improved data transfer rate.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman, Soejima et al. and AAPA and Henderson et al. before them, to include an optical link to a memory device.

The motivation for doing so would have been to avoid the mechanical degradation associated with electrical connectors **(Henderson et al. Col. 2, Lines 34-37)**.

Therefore, it would have been obvious to combine Henderson et al. with the combination of Holman, Soejima et al. and AAPA for the benefit of avoiding mechanical degradation to obtain the invention as specified in claim 22.

14. Claim 24 is rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. and AAPA as applied to claim 21 above, and further in view of Fukuda et al. (5,619,676).

Claim 24

The combination of Holman, Soejima et al. and AAPA discloses claim 21 as above.

The combination of Holman, Soejima et al. and AAPA further discloses wherein the memory device interface comprises a cache **(Holman Fig. 10, Items 1012 and 1038; Col. 11, Lines 36-40, 44-46 and 49-51)**.

The combination of Holman, Soejima et al. and AAPA does not disclose expressly wherein the performance counter is further coupled to the cache.

Fukuda et al. disclose a memory module including a cache and a counter to track the hit ratio of the cache **(Fig. 1; Abstract, Col. 7, Lines 3-9)**.

The combination of Holman, Soejima et al. and AAPA and Fukuda et al. are analogous art because they are from the similar problem solving area of improving performance of a memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman, Soejima et al. and AAPA and Fukuda et al. before them, to attach a performance counter to a cache.

The motivation for doing so would have been to improve the performance of the cache and memory **(Fukuda et al. Col. 3, Line 65 – Col. 4, Line 2)**.

Therefore, it would have been obvious to combine Fukuda et al. with the combination of Holman, Soejima et al. and AAPA for the benefit of improved cache and memory performance to obtain the invention as specified in claim 24.

15. Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. and AAPA as applied to claim 21 above, and further in view of Rotithor et al. (2004/0123043).

Claim 25

The combination of Holman, Soejima et al. and AAPA discloses claim 21 as above.

The combination of Holman, Soejima et al. and AAPA further discloses wherein the memory hub further comprises a prefetch buffer **(Holman Fig. 8, Item 812; Col. 9, Lines 59-63)**.

The combination of Holman, Soejima et al. and AAPA does not disclose expressly wherein the performance counter is further coupled to the prefetch buffer.

Rotithor et al. disclose wherein a performance couther is coupled to a prefetch buffer **(Fig. 2)**.

The combination of Holman, Soejima et al. and AAPA and Rotithor et al. are analogous art because they are from the similar problem solving area of improving performance on a memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of Holman, Soejima et al. and

AAPA and Rotithor et al. before them, to attach a performance counter to a prefetch buffer.

The motivation for doing so would have been maximizing the performance of applications **(Rotithor et al. ¶8)**.

Therefore, it would have been obvious to combine Rotithor et al. with the combination of Holman, Soejima et al. and AAPA for the benefit of improved performance of applications to obtain the invention as specified in claim 25.

16. Claim 26 is rejected under 35 U.S.C. 103(a) as being obvious over Holman in view of Soejima et al. and AAPA as applied to claim 21 above, and further in view of Battaline et al. (5,768,152).

Claim 26

The combination of Holman, Soejima et al. and AAPA discloses claim 21 as above.

The combination of Holman, Soejima et al. and AAPA does not disclose expressly wherein the memory hub further comprises a maintenance bus, and the performance counter is further coupled to the maintenance bus.

Battaline et al. disclose a system for providing performance analysis on integrated circuit devices using an IEEE JTAG 1149.1 interface **(title and abstract)**.

The combination of Holman, Soejima et al. and AAPA and Battaline et al. are analogous art because they are from the similar problem solving area of improving performance of an integrated circuit device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of he combination of Holman, Soejima et al. and AAPA and Battaline et al. before them, to incorporate a maintenance bus such as the JTAG interface into a system for performance monitoring in a memory device.

The motivation for doing so would have been to monitor the performance of the integrated circuit device without compromising the system performance **(Battaline et al. Col. 1, Lines 43-46)**.

Therefore, it would have been obvious to combine Battaline et al. with the combination of Holman, Soejima et al. and AAPA for the benefit of system monitoring without performance degradation to obtain the invention as specified in claim 26.

Relevant Art Cited by the Examiner

17. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See M.P.E.P. 707.05(c).

The following reference teaches measuring the remote request rate.

U.S. Patent/Pub. Number
2003/0056038

Conclusion

18. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

a. Per the instant office action, claims 1-34 have received a first action on the merits and are subject of a first action non-final.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ankur Gogia whose telephone number is 571-272-4166. The examiner can normally be reached on M-F 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ankur Gogia
Examiner
Art Unit 2187

1/20/2006

CHRISTIAN CHACE
PRIMARY EXAMINER